Atty. Dkt. No.: 39153/649 (H0982)

**U.S. PATENT APPLICATION**

**for**

# FULLY DEPLETED STRAINED SILICON ON INSULATOR TRANSISTOR AND METHOD OF MAKING THE SAME


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# FULLY DEPLETED STRAINED SILICON ON INSULATOR TRANSISTOR AND METHOD OF MAKING THE SAME

## FIELD OF THE INVENTION

**[0001]** The present invention relates to integrated circuit (IC) devices. More particularly, the present invention relates to a strained silicon structure on an insulator substrate.

## BACKGROUND OF THE INVENTION

**[0002]** Semiconductor devices such as processors, non-volatile memory, and other circuits include semiconductor elements such as metal oxide semiconductor field effect transistors (MOSFETS), diodes, resistors, and capacitors. For example, flash memory devices employ millions of floating gate FETs and processors employing millions of complementary MOSFETS. MOSFETS are generally disposed in active regions disposed in a base layer or substrate. Active regions typically include heavily doped silicon or other semiconductor regions. The regions can be doped with impurities such as phosphorous (P), boron (B), arsenic (As), or other impurities.

**[0003]** Semiconductor elements such as floating gate transistors and FETs are generally bulk semiconductor-type devices in contrast to semiconductor-on-insulator-type devices such as silicon-on-insulator (SOI) devices. The floating gate transistors and FETs are disposed in a single plane (e.g., a single active layer) on a top surface of a semiconductor substrate such as a single crystal silicon substrate.

**[0004]** Semiconductor-on-insulator (SOI) (e.g., silicon-on-insulator) devices have significant advantages over bulk semiconductor-type devices, including near ideal subthreshold voltage slope, elimination of latch-up, low junction capacitance, and effective isolation between devices. SOI-type devices generally completely surround a silicon or other semiconductor substrate with an insulator. Devices such as conventional FETs or other transistors are disposed on the silicon substrate by doping source and drain regions and by providing gate conductors between the source and drain regions. SOI devices provide significant advantages, including reduced chip size or increased chip density because minimal device separation is needed due to the surrounding insulating layers. Additionally, SOI devices can operate at increased speeds due to reduction in parasitic capacitance. These advantages are particularly important as integration technologies reach sub-100 nanometer levels for CMOS devices.

**[0005]** Conventional SOI devices generally have a floating substrate (i.e., the substrate is often totally isolated by insulating layers). SOI devices can be subject to floating substrate effects, including current and voltage kinks, thermal degradation, and large threshold voltage variations. Generally, SOI devices can include a very thin (200-800 Å thick) silicon film separated from a bulk substrate by a thick buried oxide (e.g., a 2000-3000 Å thick BOX layer).

**[0006]** Strained silicon (SMOS) processes are utilized to increase transistor (e.g., MOSFET) performance by increasing the carrier mobility of silicon, thereby reducing resistance and power consumption and increasing drive current, frequency response and operating speed. Strained silicon is typically formed by growing a layer of silicon on a silicon

germanium substrate or layer. Germanium can also be implanted, deposited, or otherwise provided to silicon layers to change the lattice structure of the silicon and increase carrier mobility.

**[0007]** The silicon germanium lattice associated with the germanium substrate is generally more widely spaced than a pure silicon lattice, with spacing becoming wider with a higher percentage of germanium. Because the silicon lattice aligns with the larger silicon germanium lattice, a tensile strain is created in the silicon layer. The silicon atoms are essentially pulled apart from one another. Relaxed silicon has a conductive band that contains six equal valance bands. The application of tensile strength to the silicon causes four of the valance bands to increase in energy and two of the valance bands to decrease in energy. As a result of quantum effects, electrons effectively weigh 30 percent less when passing through the lower energy bands. Thus, lower energy bands offer less resistance to electron flow.

**[0008]** In addition, electrons meet with less vibrational energy from the nucleus of the silicon atom, which causes them to scatter at a rate of 500 to 1,000 times less than in relaxed silicon. As a result, carrier mobility is dramatically increased in strained silicon compared to relaxed silicon, providing an increase in mobility of 80 percent or more for electrons and 20 percent or more for holes. The increase in mobility has been found to persist for current fields up to 1.5 megavolt/centimeter. These factors are believed to enable device speed increase of 35 percent without further reduction of device size, or a 25 percent reduction in power consumption without reduction in performance.

[0009] Heretofore, it has been difficult to manufacture SMOS devices on SOI substrates. Generally, providing a suitable strained silicon layer above an insulative substrate to achieve the advantage of an SOI substrate can be problematic. In addition, providing a strained silicon layer thin enough for a fully depleted MOSFET above an insulative layer can be difficult using conventional processes. A fully depleted MOSFET is a transistor for which the depletion region encompasses the entire or nearly the entire channel region.

[0010] Thus, there is a need for an SOI and strained semiconductor device. Further, there is a need for an SOI device which includes a strained silicon layer. Further still, there is a need for method of manufacturing an SOI structure including a strained silicon layer. Yet further, there is a need for a fully depleted transistor which has some of the advantages of SOI devices and SMOS devices. Even further, there is a need for an efficient method of manufacturing an SMOS device on an insulative substrate. Further still, there is a need for an efficient process for fabricating fully depleted SMOS SOI transistors.

## SUMMARY OF THE INVENTION

[0011] An exemplary embodiment relates to an integrated circuit. The integrated circuit includes a first wafer including a silicon germanium layer, a strained silicon layer, and a first insulating layer. The integrated circuit also includes a second wafer including a substrate and a second insulating layer. The second insulating layer is attached to the first insulating layer.

[0012] Another exemplary embodiment relates to a multi-layer structure containing a plurality of SMOS transistors. The multi-layer structure includes a semiconductor/germanium layer, a strained semiconductor layer below the semiconductor germanium layer, a gate dielectric, and a gate conductor. The strained semiconductor layer is below the semiconductor/germanium layer. The semiconductor/ germanium layer includes an aperture. The gate dielectric is above the strained semiconductor layer and within the aperture, and the gate conductor is also within the aperture. The strained semiconductor layer includes a source and a drain.

[0013] Still another exemplary embodiment relates to a method of making an SMOS structure containing a plurality of transistors. The method includes providing a first semiconductor substrate including a base layer, a strained semiconductor layer, and a first oxide layer. The method also includes attaching a second semiconductor substrate including a second oxide layer to the first oxide layer and separating the base layer from the first substrate.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Exemplary embodiments will hereafter be described with reference to the accompanying drawings, wherein like numerals denote like elements, and:

[0015] FIGURE 1 is a flow diagram showing a process for fabricating a device such as a fully depleted SMOS transistor on an insulator substrate;

**[0016]** FIGURE 2 is a cross-sectional view schematic drawing of a portion of an IC substrate used in the process illustrated in FIGURE 1, the IC substrate including a strained silicon layer above a silicon germanium layer;

**[0017]** FIGURE 3 is a cross-sectional view of a portion of another IC substrate used in the process illustrated in FIGURE 1;

**[0018]** FIGURE 4 is a cross-sectional view of the portion illustrated in FIGURE 3, showing a step that combines the portion illustrated in FIGURE 2 with the portion illustrated in FIGURE 3;

**[0019]** FIGURE 5 is a cross-sectional view of the portions illustrated in FIGURE 4, showing a layer removal step;

**[0020]** FIGURE 6 is a cross-sectional view of the portion illustrated in FIGURE 5, showing the portions flipped from the orientation illustrated in FIGURE 5;

**[0021]** FIGURE 7 is a cross-sectional view of the portions illustrated in FIGURE 6, showing an etching step;

**[0022]** FIGURE 8 is a cross-sectional view of the portions illustrated in FIGURE 7, showing a doping step;

**[0023]** FIGURE 9 is a cross-sectional view of the portions illustrated in FIGURE 8, showing a spacer formation step;

**[0024]** FIGURE 10 is a cross-sectional view of the portions illustrated in FIGURE 9, showing a gate dielectric and gate conductor provision step;

**[0025]** FIGURE 11 is a cross-sectional view of the portions illustrated in FIGURE 10, showing a polishing step; and

**[0026]** FIGURE 12 is a cross-sectional view of the portions illustrated in FIGURE 11, showing a silicidation step.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

**[0027]** With reference to FIGURES 1 and 12, a portion of a multilayer integrated circuit 12 (FIGURE 1) includes a structure 15 and a structure 11 manufactured in a process 100. In one embodiment, process 100 forms transistors in a semiconductor/germanium layer (e.g., a silicon/germanium layer) and a strained silicon layer. A gate conductor is provided in an aperture in the semiconductor/germanium layer. The strained layer can be doped through the aperture in the semiconductor/ germanium layer. The strained layer is disposed above an insulating substrate or buried oxide (BOX) layer.

**[0028]** Integrated circuit 12 (Figure 12) is preferably a strained semiconductor (SMOS) semiconductor-on-insulator (SOI) device. Structure 11 preferably includes a transistor (e.g., a fully depleted field effect transistor or FD MOSFET). Structure 15 supports structure 11 and is provided below structure 11.

**[0029]** Structure 11 can be built on a bulk substrate including germanium, a semiconductor bulk substrate, or another IC substrate. Structure 11 preferably includes a strained semiconductor layer, such as a strained silicon layer 16.

**[0030]** Structure 15 includes a support substrate 19 and an insulating layer 21. Support substrate 19 can be a silicon substrate that along with layer 21 assists the formation of the SOI structure of integrated circuit 12.

**[0031]** Integrated circuit 12 can include a semiconductor device or portion thereof made from any of the various semiconductor processes such as a complementary metal oxide semiconductor (CMOS) process or any other semiconductor process. The portion of integrated circuit 12 shown in FIGURE 12 may be an entire IC or a portion of an IC and may include a multitude of electronic components. Devices and interconnections for integrated circuit 12 can be located on structures 11 and 15 as well as on additional layers provided on structures 11 and 15.

**[0032]** Structure 11 includes a silicon/germanium layer 14, (e.g., a semiconductor/germanium layer), a strained semiconductor layer 16 (e.g., a strained silicon layer), and an insulating layer 17. Insulating layer 17 of structure 11 and insulating layer 21 of structure 15 are preferably bonded together at an interface represented by a dotted line between layers 17 and 21.

**[0033]** Process 100 can be utilized to form integrated circuit 12. According to process 100, structure 11 is formed including strained silicon layer 16 and silicon germanium layer 14 in a step 49. In a step 54, structure 15 is provided. Structure 15 can be comprised of a handle wafer substrate such as substrate 19. Insulating layer 21 can be grown or deposited upon substrate 19. Similarly, an insulative layer 17 can be grown upon layer 21. Alternatively, substrate 19 and structure 11 can be purchased with respective layers 17 and 21 already formed.

**[0034]** In a step 56, structures 11 and 15 are coupled together to form a compound multilayer structure in a step 56. Preferably, layers 17 and 21 are bonded by any known technique, such as a hydrogen bonding technique. Advantageously, structure 11 includes strained silicon layer 16 above insulative layers 17 and 21, thereby providing the advantages of SMOS and SOI processes.

**[0035]** In a step 58, support layers and other unnecessary layers associated with structure 11 can be removed from a top surface of layer 14. In a step 60, an aperture can be etched through layer 14 to form a gate structure. In a step 62, layer 16 can be doped to form source and drain extensions through the aperture associated with the gate structure. In a step 64, a gate structure 37 can be provided in the aperture.

**[0036]** With reference to FIGURE 12, various processes can be utilized to form various structures for integrated circuit 12. In one embodiment, integrated circuit 12 can include silicided source and drain regions 22 and 24 and source and drain extensions 23 and 25. Source and drain regions 22 and 24 associated with layer 14 as well as a gate conductor 46 can be silicided to form silicided regions 48 and 49, respectively. Preferably, insulative spacers 35 and a gate structure 37 can be formed in the aperture.

**[0037]** The transistor associated with source and drain regions 22 and 24 preferably is fully depleted so that the depletion region extends through the entire thickness of layer 16. Gate structure 37 between source and drain regions 22 and 24 includes a gate conductor 46 and a gate dielectric 47.

**[0038]** Gate dielectric 47 is preferably 5-30 Angstroms thick. Gate dielectric 47 can be silicon dioxide ($SiO_2$), silicon nitride ($Si_3N_4$) or a high-k dielectric material.

**[0039]** Gate conductor 46 is surrounded by dielectric spacers 35. Gate conductor 46 can be a metal or doped polysilicon material. Dielectric spacers 35 can be comprised of a silicon dioxide or silicon nitride material.

**[0040]** Source and drain regions 22 and 24 preferably extend through the entire thickness of layer 16. Source region 22 and drain region 24 are preferably 100-200 Angstroms deep preferably formed by ion implantation. Extensions 23 and 25 are not necessary in the fully depleted embodiment of the transistor. Regions 22 and 24 can have a concentration of between approximately $10^{19}$ to $10^{21}$ dopants per $cm^3$. The dopants can include boron (B), arsenic (As), phosphorous (P), boron difluoride ($BF_2$), etc.

**[0041]** Referring to FIGURES 2 through 12, a cross-sectional view of the portion of integrated circuit (IC) 12 is illustrated. Integrated circuit 12 is subjected to process 100 (FIGURE 1) to form an IC including at least one transistor. Integrated circuit 12 can include a multitude of fully depleted SMOS, SOI transistors with a gate structure 37 and silicided source and drain regions 22 and 24 fabricated as explained below.

**[0042]** In FIGURE 2, multilayer structure 11 is a provided as an integrated circuit wafer including a strained layer such as strained silicon layer 16 provided over a semiconductor/germanium layer such as silicon/germanium layer 14. Layer 14 can be provided above a substrate 13.

**[0043]** Substrate 13 is optional and integrated circuit 12 can be provided with layer 14 as the bottom-most layer. Substrate 13 can be the same material or a different material than layer 14. In one embodiment, substrate 13 is a semiconductor substrate, such as a silicon substrate upon which layer 14 has been grown.

**[0044]** Silicon/germanium layer 14 is preferably a silicon germanium or other semiconductor material including germanium, and can be doped with P-type dopants or N-type dopants. Layer 14 can be an epitaxial layer provided on a semiconductor or an insulative base, such as substrate 13. Furthermore, layer 14 is preferably a composition of silicon germanium ($Si_{1-x}$ $Ge_x$, where X is approximately 0.2 and is more generally in the range of 0.05-0.3). Layer 14 can be grown or deposited.

**[0045]** In one embodiment, layer 14 is grown above substrate 13 by chemical vapor deposition (CVD) using disilane ($Si_2H_6$) and germane ($GeH_4$) as source gases with a substrate temperature of approximately 650°C, a disilane partial pressure of approximately 30 mPa and a germane partial pressure of approximately 60 mPa. Growth of silicon germanium material may be initiated using these ratios, or, alternatively, the partial pressure of germanium may be gradually increased beginning from a lower pressure or zero pressure to form a gradient composition. Alternatively, a silicon layer can be doped by ion implantation with germanium or by another process to form layer 14. Preferably, silicon/germanium layer 14 is grown by epitaxy to a thickness of less than approximately 5000 Å (and preferably between approximately 1500 Å and 4000 Å).

**[0046]** Strained silicon layer 16 is formed above layer 14 by an epitaxial process. Preferably, layer 16 is grown by chemical vapor

deposition (CVD) at a temperature of approximately 650°C using silane or dichlorosilane. Layer 16 can be a pure silicon layer and have a thickness of 100-200 Å. Layer 14 maintains the strained nature of layer 16 throughout process 100.

**[0047]** Layers 14 and 16 can include isolation regions which separate active regions for transistors on structure 11. Isolation regions can be insulating regions such as silicon dioxide regions formed in conventional local oxidation of silicon (LOCOS) processes. Alternatively, isolation regions can be formed in a shallow trench isolation (STI) process.

**[0048]** Structure 11 can include an insulating layer 17. Insulating layer 17 is preferably a thermally grown or deposited silicon dioxide layer having a thickness of approximately 200-400 Å. In an alternative embodiment, layer 17 can be deposited as high-temperature oxide or in a tetraethylorthosilicate (TEOS) based process. In another alternative, layer 17 can be formed in an oxygen ion implantation process. Layer 17 is preferably utilized in the bonding technique associated with step 56 of process 100.

**[0049]** In FIGURE 3, multilayer structure 15 is provided in accordance with step 54 of process 100. In one embodiment, structure 15 includes a handle wafer or substrate 19 and an insulating layer 21. Preferably, substrate 19 is a silicon material and layer 21 is a silicon dioxide material similar to layer 17. Layer 21 can be formed in a process similar to the process used to form layer 17 (FIGURE 2). In one embodiment, structure 15 is a conventional handle wafer and is 100 microns thick and layer 21 is 200-400 Å thick.

**[0050]** In FIGURE 4, structure 11 is bonded to structure 15 in step 56. In a preferred embodiment, layer 17 of structure 11 is bonded to layer 21 of structure 15 at an interface represented by a dashed line. Any of a variety of attachment or bonding techniques can be utilized to form integrated circuit 12 including structures 11 and 15.

**[0051]** In FIGURE 4, structure 15 is inverted or flipped over with respect to its orientation shown in FIGURE 3. Preferably, structure 15 is flipped top over bottom with respect to its orientation in FIGURE 5 so that insulating layer 21 contacts insulating layer 17 of structure 11.

**[0052]** Preferably, wafer bonding (bonding of structures 11 and 15) is completed at room temperature and in a nitrogen ($N_2$) ambient atmosphere in step 56. The wafer bonding is completed by atomic force. Alternatively, higher temperatures can be utilized during bonding.

**[0053]** In one embodiment, Smart-Cut® and Unibond® techniques can be utilized to bond structures 11 and 15. Smart-Cut® and Unibond® techniques are discussed in "Smart-Cut®: The Basic Fabrication Process for UNIBOND® SOI Wafers," by Auberton-Herue, Bruel, Aspar, Maleville, and Moriceau (IEEE TRANS ELECTRON, March 1997), incorporated herein by reference. The Smart-Cut® and Unibond® techniques can reach temperatures of 110°C to bond layers 17 and 21 together.

**[0054]** The Smart-Cut® and UNIBOND® techniques utilize a combination of hydrogen implantation and wafer bonding to form an SOI substrate. Applicants have modified the techniques to attach a strained silicon layer containing structure (structure 11) to a handle wafer (structure 15) to form a strained silicon on SOI layer. OH terminated clean oxide

surfaces on layers 17 and 21 in hydrophilic conditions can be used to bond structures 11 and 15. Hydrogen bonding at the surfaces is achieved through water adsorption.

**[0055]** Alternative techniques for attaching wafers can be utilized without departing from the scope of the claims. For example, structures 11 and 15 can be bonded by an adhesive or other chemical means.

**[0056]** In FIGURE 5, after structures 11 and 15 are bonded, layer or substrate 13 of structure 11 is removed in step 58. Removal of layer substrate 13 leaves layers 14, 16 and 17 attached to structure 15. A mechanical process can be utilized to cleave substrate 13 from layer 14. The process leaves layer 14 as the top (exposed) surface of layer 16. Alternatively, substrate 13 can be removed by polishing or etching.

**[0057]** In one embodiment, a hydrogen breaking interface can be formed at the interface of layer 14 and substrate 13 or within a bottom portion of layer 14. The hydrogen breaking interface can be used to separate substrate 13 from layer 14 in a Smart-Cut® process.

**[0058]** FIGURE 6 shows integrated circuit 12 inverted or flipped from its orientation shown in FIGURE 5. In FIGURE 6, integrated circuit 12 includes layer 14 above layer 16, and structure 11 above structure 15.

**[0059]** In FIGURE 7, an aperture 72 is formed in layer 14 in accordance with step 58. In a preferred embodiment, aperture 72 is formed in a photolithographic process. Aperture 72 preferably has a width of 2000 A depending upon desired gate length and a depth equal to that of layer 14.

In one embodiment, aperture 72 can be less than 500 A Angstroms deep formed by dry etching. In another embodiment, aperture 72 can extend into layer 16. Various etching processes selective to layer 14 can be utilized.

**[0060]** In one embodiment, an etching process which monitors the presence of germanium in etching byproducts is utilized. The reduction of the presence of germanium in the etching byproducts indicates that layer 16 has been reached (i.e., layer 16 does not include significant amounts of germanium). The etching process is preferably selective to silicon germanium with respect to silicon at a 2:1 ratio. The etching processes can be $CF_4$, $SF_6$, $CF_2CL_2$, HBr, and $SF_6/H_2/CF_4$ processes (preferably $CF_4$ and $SF_6$ processes).

**[0061]** In FIGURE 8, layer 16 is doped by an ion implantation to form source and drain regions 22 and 24. In another embodiment, source and drain regions can be provided during any part of process 100. Alternatively, layer 16 and layer 14 can be doped for regions 22 and 24 by other techniques.

**[0062]** Layer 14 serves as a mask for the appropriate formation of extensions 23 and 25. In one embodiment, an angled dopant extension implant 32 can be utilized. Preferably, dopants are accelerated at an energy of 1 X 10 keV at an angle of 15-45 and a dose of 14-15 through aperture 72. Alternative methods can be utilized to form extensions 23 and 25. The dopants can be B, P, As, $BF_2$, Sb, etc.

**[0063]** According to an alternative embodiment, spacers similar to spacers 35 can include dopants which are driven into extensions 23 and 25. In yet another embodiment, source and drain regions 22 and 24

and extensions 23 and 25 can formed by a conventional doping process before aperture 72 is formed.

**[0064]** In FIGURE 9, spacers 35 are formed in aperture 72. Preferably, a deposition and etch-back process is utilized to form spacers 35. Spacers 35 can be formed by depositing silicon nitride or silicon dioxide material and etching in an anisotropic dry etch process. Preferably, an aperture 74 exists between spacers 35. Spacers 35 can have a width of 500 A and a height of 300-500 A. Preferably, spacers 35 have an initial height that is the same height as layer 14.

**[0065]** In FIGURE 10, a gate dielectric layer 47 is provided in aperture 74. Gate dielectric layer 47 can be a thermally grown silicon nitride layer or a thermally grown silicon dioxide layer. In another embodiment, layer 47 is deposited and etched at an angle to leave layer 47 at the bottom of aperture 74. Alternative processes can be utilized for forming layer 47 in aperture 74. Layer 47 can also be a high-k dielectric layer.

**[0066]** In FIGURE 10, aperture 74 is filled with a conducting material 45 for gate conductor 46 in accordance with step 64 of process 100. Preferably, conducting material 45 is deposited as a conformal layer of polysilicon or metal material. In one embodiment, conducting material 45 is a metal material having different etch properties than layer 14. In another embodiment, a hard mask layer or barrier, buffer layer, or combination of both is provided between layer 14 and conducting material 45.

**[0067]** In FIGURE 11, conducting material 45 is removed from above layer 14 to complete gate structure 37. In FIGURE 12, layer 14 is etched or otherwise partially removed to lower its top surface below a top

surface of gate conductor 46. After lowering the top surface of layer 14, layer 14 above source region 22 and drain region 24 can be silicided to form silicide regions 48. In addition, gate conductor 46 can be silicided to form silicide region 49. Preferably, a nickel silicidation process is utilized. Nickel material is sputter deposited and annealed to form regions 48 and 49. Various techniques and various materials can be utilized to form silicide regions 48 and 49.

**[0068]** An insulating layer can be deposited above integrated circuit 12 shown in FIGURE 12. Various interconnection processes and interconnect layers can be utilized to provide circuitry associated with integrated circuit 12.

**[0069]** With reference to FIGURE 6, in an alternative embodiment of process 100, an etch stop layer such as silicon nitride can be provided above layer 14. In FIGURE 7, aperture 72 is provided through the etch stop layer as well as layer 14.

In FIGURE 9, spacers 35 are formed in aperture 72. Spacers 35 in this alternative embodiment are formed such that the top of spacers 35 is coplanar with the top of the etch stop layer above layer 14. The etch stop layer provides an additional advantage of allowing spacers to be polished back until the etch stop layer is reached.

In FIGURE 11, conducting material 45 for gate conductor 46 is deposited over the etch stop layer and polished until the etch stop layer is reached, thereby leaving gate conductor 46 in aperture 74. After polishing material 45, the etch stop layer can be removed in a conventional stripping process, thereby leaving spacers 35 above a top surface associated with

layer 14. Such an alternative process allows spacers 35 to more adequately insulate gate conductor 46 from layer 14.

**[0070]** It should be understood that the detailed drawings and specific examples describe exemplary embodiments of the present invention and are provided for the purpose of illustration only. The apparatus and method of the invention is not limited to the precise details, geometries, dimensions, materials, and conditions disclosed. For example, although particular layers are described as being particular sizes, other sizes can be utilized. Further still, although polysilicon is used as a gate conductor, other conductor materials can be utilized. Even further still, the drawings are not drawn to scale. Various changes can be made to the precise details discussed without departing from the spirit of the invention which is defined by the following claims.